Self-Heating Effect in a 65nm MOSFET at Cryogenic Temperatures

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***Abstract*— We characterized the thermal behavior of a 65 nm bulk-CMOS transistor, by measuring the self-heating effect (SHE) as a function of the bias condition. We demonstrated that at the base temperature of 6.5 K the channel temperature of the transistor can increase up to several tens of Kelvins due to power dissipation. The thermal behavior of the transistor is determined not only by the thermal response of the transistor itself, but also by the thermal properties of the surroundings, i.e., the source, drain, bulk and gate interfaces, the metal contacts and vias. On top of it, the thermal response is bias dependent through the bias dependence of power and self-heating. This information becomes relevant for the proper design of integrated circuits for quantum computing or other cryogenic applications, where the circuitry requires to be operated at a stable cryogenic temperature.**

***Index Terms*— CMOS, Cryogenic temperature, Quantum Computing, Self-heating**

I. Introduction

COMPLEMENTARY metal–oxide–semiconductor technology (CMOS) in cryogenic environments is a trending topic for the last decade. First low-temperature measurements of CMOS field-effect transistors (MOSFETs) were published in 1968 [1], [2], and interest in this topic has recently increased due to new cryogenic applications, such as outer-space devices, scientific instruments [3] and particularly quantum computing [4], [5]. The increasing number of qubits in quantum systems created the necessity of hardware, which is able to work in deep cryogenic temperatures. Along with several types of superconducting logic, CMOS integrated circuits seem to be a good candidate for this purpose, due to large experience in design and fabrication. Highly integrated system-on-chip solutions can be used as control and readout electronic systems for several types of qubits, providing the opportunity to scale up the number of qubits in quantum information processors [6]. Some of the design concepts even propose the placement of control electronics together with the qubit array on the same die [7].

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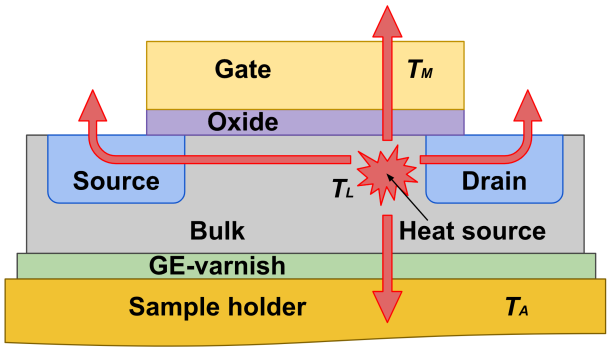

Fig. 1: The four thermal paths of the n-type transistor.

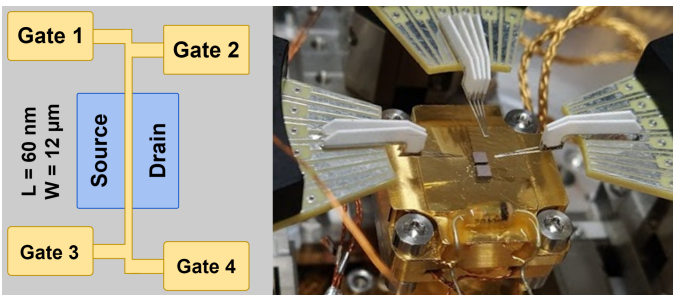

Fig. 2: Layout scheme of the measured sample (left) and a photo of the working area of the setup (right).

However, as already reported by several authors [8]–[11], the presence of various scattering processes self-heats the transistor and makes its temperature different from that of the cryogenic environment, which should be accounted for the development of the proper cryogenic process design kit (PDK). Moreover, self-heating is not taken into account in most of the literature on cryogenic effects research in CMOS devices. The local heating influences the behavior of the device itself, as well as the behavior of other thermally connected devices. In case of quantum computing, electro-thermal effects in the CMOS could severely degrade the performance of the qubits or even render them unusable.

Therefore, understanding the way heat is generated in the active region of the transistor and how it diffuses away from the hot spot through the different thermal paths, becomes

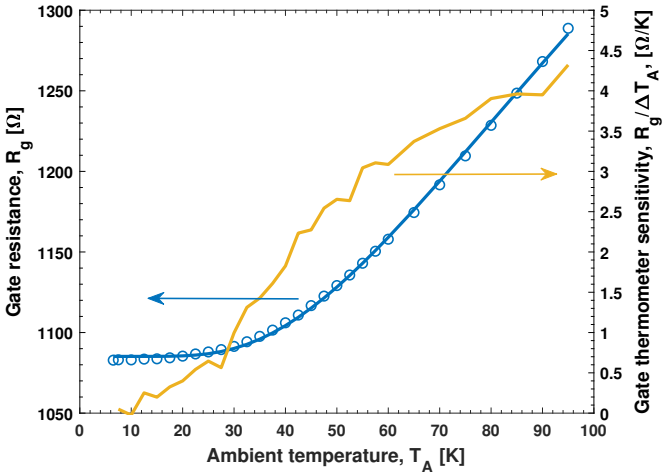

Fig. 3: Measured gate resistance R_g at different ambient temperatures T_A, fitted with Fermi-like function (left Y axis) and gate resistance thermometer sensitivity (right Y axis).

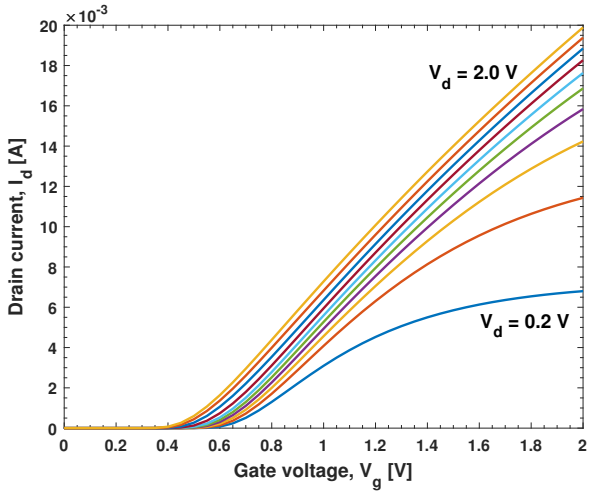

Fig. 4: Measured $I_d - V_g$ characteristics with V_d as a parameter at T_A = 6.5 K. V_d step size is 0.2 V.

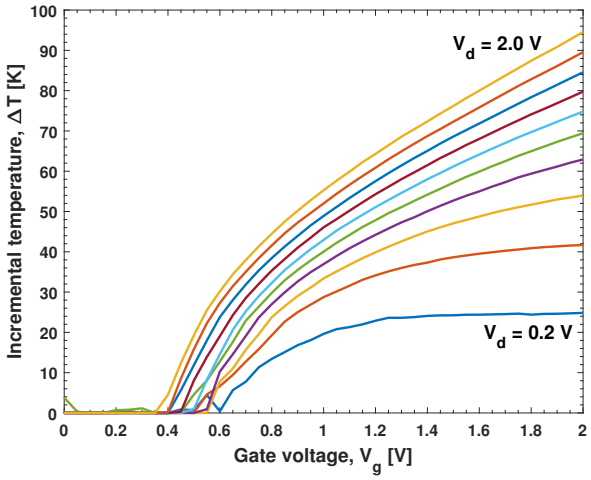

Fig. 5: Measured incremental temperature ΔT versus V_g with V_d as a parameter at T_A = 6.5 K. V_d step size is 0.2 V.

essential for the design of high perfomance integrated circuits for cryogenic applications and the overall system design.

The purpose of our work is to investigate self-heating effect (SHE) in 65-nm bulk CMOS technology. With the use of the gate resistance thermometer technique, we have investigated thermal properties of the transistor and its surroundings. From the experimental data we also describe qualitatively the contribution of different thermal paths to the electro-thermal behavior of the transistor. A quantitative description would require the design of special test structure, with different geometries that allow for a quantitative thermal de-embedding.

II. Device Technology and Experimental Setup

Thermal behavior of a MOSFET is explained by the interplay of electrical and thermal parameters, such as Joule power P dissipated by the device, thermal resistance R_{th} and thermal capacitance C_{th}, surrounding the active region of the transistor. If we consider a static system where the transient thermal effects are neglected, then because of carrier scattering [12] in the active channel, most of the carrier energy is transferred to the lattice, which then translates into an increase of the local temperature T_L [13]. This is known as the self-heating effect [14]. As the Joule power is a function of the bias conditions, such as drain current I_d, gate voltage V_g, and drain voltage V_d, then T_L also becomes a function of the bias conditions. The thermal equilibrium of the transistor is reached when the cooling power, determined by temperature difference and thermal conductivity through the 4 different paths (as shown in Fig. 1), is equal to the self-heating power.

At this point, the differential temperature ΔT is defined by the temperature drop across the four thermal paths: $\Delta T = (T_L - T_A)$. Therefore, a way to indirectly measure T_L is by setting a thermometer as close as possible to the hot spot in the active channel. For that purpose, in this experiment we design a gate resistor thermometer [15], configured as a 4-terminal device as shown in Fig. 2, left. The self-heating structure was designed and fabricated in 65 nm CMOS technology by TSMC, with gate oxide thickness T_{ox} = 1.9 nm. The poly-silicon gate is used as a thermometer which is as close as possible to the source of heat produced in the active channel of the transistor. The selfheating test structure has (W/L) = 12 µm / 60 nm geometry. As a matter of experimental demonstration we introduce results for a n-type 65 nm MOSFET, which can be later expanded for the p-type device.

The gate of the test transistor with its four contacts (Fig. 2, left) is used to calibrate the gate resistance as a function of the temperature, which is measured with the transistor in off mode. We used a closed-cycle cryostat attocube attoDRY800 with DC probing configuration (Fig. 2, right). The sample was glued to the sample holder with thermally conductive GE-varnish. The sample holder has a temperature sensor and a heater close to the sample area to control the holder's temperature. The Keysight B1500A Semiconductor Device Analyzer was used for all the DC measurements.

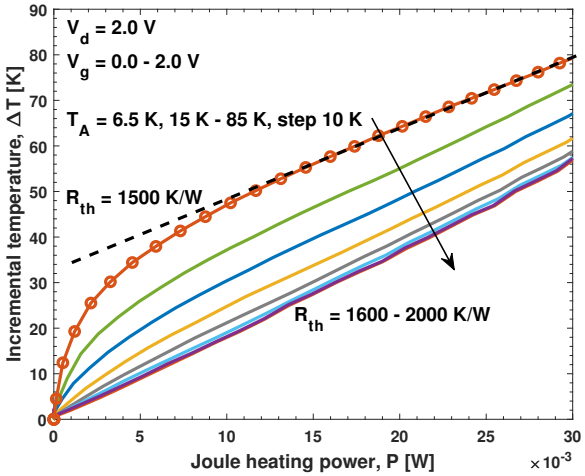

Fig. 6: Measured incremental temperature ΔT versus Joule power P for V_d = 2.0 V at several ambient temperature T_A values.

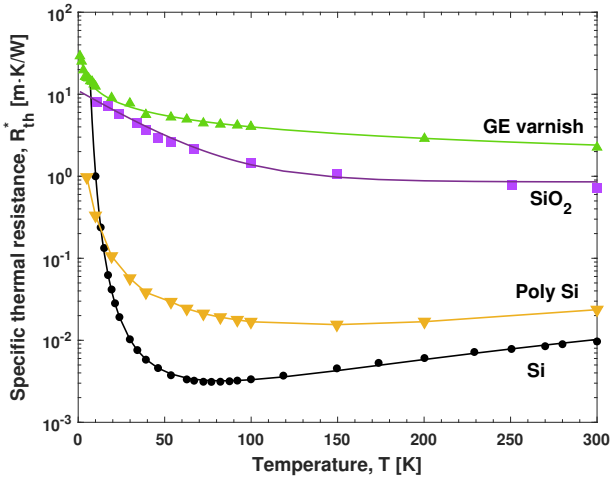

Fig. 7: Specific thermal resistance R^*_{th} versus temperature for different materials [17]–[22].

We performed a temperature-controlled measurement of the gate resistance dependence with respect to the base temperature (see Fig. 3). Using the four-terminal sensing technique, we apply a potential difference of 20 mV to the ends of the gate and measure the current. This approach provided a minor influence on the transistor behavior and negligible polysilicon gate self-heating, as the Joule heating power dissipation during resistance measurements is less than 400 nW. The measured data is fitted to a Fermi-like function (eq.1, [11]) in the 6.5 K – 95 K temperature range, as shown in Fig. 3.

III. Experimental Results and Analysis

The experimental data in Fig. 3 shows that the polysilicon resistance R_g is almost constant for temperatures below about 15 K, which is a result of residual impurity scattering, due to metallic behavior of polysilicon versus temperature [16]. As the resistance measurement accuracy in this range is 0.3 Ohm, data for channel temperatures lower than 15 K is not reliable. We set a time of 1 s before each measurement point in order to achieve thermal equilibrium over the whole chip. The $I_d - V_g$ characteristics with V_d as a parameter are shown in Fig. 4.

The transistor handles I_d up to 20 mA, which is equivalent to a heating power P of 40 mW, at $V_g = V_d = 2.0\ V$. As seen from the Fig. 4 and 5, ΔT is a function of I_d, V_g, and V_d. For $V_g = V_d = 2.0\ V$ condition ΔT raises up to 94 K. Plotting the incremental temperature ΔT versus the Joule power (I_d times V_d) gives a better perspective, as it is related to the thermal properties, like the thermal resistance R_{th} (Fig. 6, marked line).

The $\Delta T - P$ curve for $V_d = 2.0\ V$ with V_g sweeping from 0.0 to 2.0 V in Fig. 6 shows two regions: a nonlinear region for low Joule power magnitudes, and a linear region for high Joule power ones. Incremental temperature ΔT is related to the Joule power through the thermal resistance R_{th} as described by equation:

$$\Delta T = R_{th} \cdot P \tag{1}$$

Fig. 7 allows for better understanding of the thermal performance, which is based on the temperature dependence of the thermal resistance. The data shown in Fig. 7 has been replotted and fitted from various references [17]–[22]. Because of the presence of SiO_2, the heat flow sees a higher thermal resistance when flowing from the hot spot towards the SiO_2. GE-varnish, which was used to glue the Si die to the cold plate, has higher thermal resistivity than Si, but large thermal contact area and small thickness of the varnish layer makes this path relatively high thermally conductive. The heat, generated at the active region of the channel, flows through the bulk and lateral paths of the drain and source, then through the vias and metal interconnects (Fig. 1). Under this thermal scenario, the thermal resistance of Si dominates the heat flow. In turn, any increase of temperature in the transistor will dramatically reduce the thermal resistance of Si by several orders of magnitude. The experimental data in Fig. 6 shows the temperature raise from the 6.5 K cold-plate value up to about 100 K. Thus, the Si specific thermal resistance R^*_{th} swings from about 30 m·K/W down to 0.004 m·K/W (Fig. 7). This enables heat flow from the transistor channel through the Si out through the source/drain contacts and varnish layer, leading to a thermalization of the transistor.

The profile of the $R_{th} - T$ curve for Si, SiO_2, and poly-Si (Fig. 7) is a function of doping profile and sample thickness [17], [20], [23]–[25]. Therefore, the magnitude varies according to thickness and doping or composition in the case of poly-Si and SiO_2. In the case of Si, the minimum value R_{th} happens at about T = 75 K and moves to a lower or higher temperature, depending on the doping concentration. The higher Si doping concentration, the higher the magnitude of the thermal resistance and the higher the temperature at which it reaches its minimum value or inflexion point [26].

In order to prove the Si thermal resistance domination over the other thermal components, the experiment was repeated for several higher temperatures, including T_A = 75 K, which is the temperature at which R_{th} gets its minimum value and has an inflexion point. The incremental temperature ΔT versus

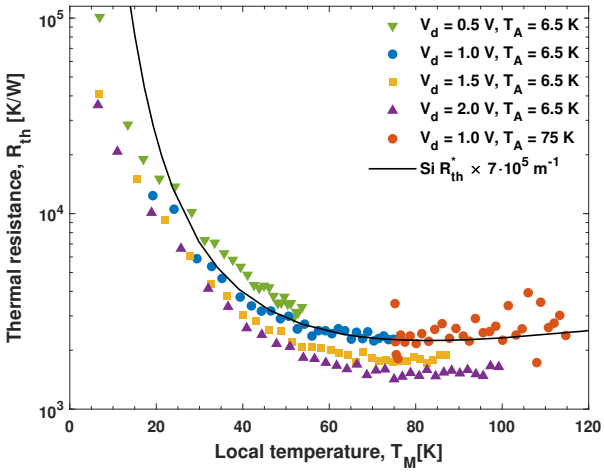

Fig. 8: Extracted thermal resistance R_{th} seen from the gate side as a function of the temperature T_M measured at the gate, for V_d of 0.5, 1.0, 1.5 and 2.0 V at T_A = 6.5 K and for V_d = 1.0 V at T_A = 75 K.

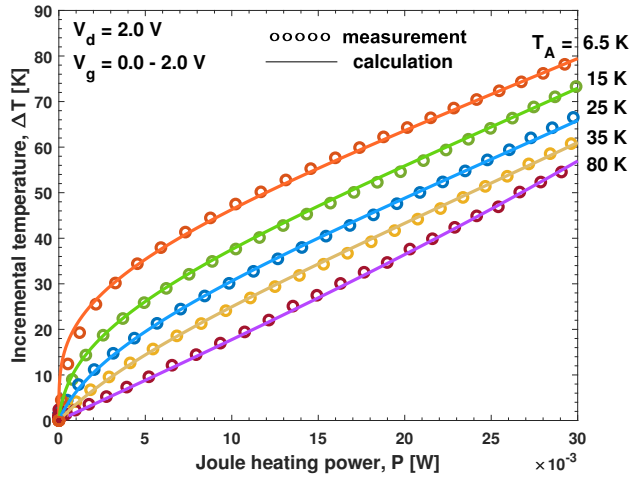

Fig. 9: Calculated and measured channel temperature increase as a function of the dissipated power for several T_A.

the Joule power for V_d = 2.0 V and V_g swept from 0.0 to 2.0 V is shown in Fig. 6. Starting from T_A = 60 K the $\Delta T - P$ relationship is almost linear with a slight second-order polynomial behavior. The derivatives $(d\Delta T/dP)$ of lines for T_A higher then 60 K give a thermal resistance R_{th} of 1600-2000 K/W. This result indicates that R_{th}, measured at the gate at temperatures close to 75 K, changes slightly, which is consistent with Fig. 7. Because of the increased thermal resistance of silicon, the SHE effect is more pronounced at T_A lower then 60 K, remaining almost constant as the T_A rises.

The plot of the derivative $(d\Delta T/dP)$ versus the measured temperature at the gate for both T_A = 6.5 K and 75 K, is shown in Fig. 8. The data at T_A = 6.5 K is given for V_g sweep and V_d equal 0.5, 1.0, 1.5 and 2.0 V; the data at T_A = 75 K is given for V_d = 1.0. Solid line is calculated from the specific thermal resistance R^*_{th} curve for Si (Fig. 7), with the assumption that effective length versus effective area ratio is $7{\cdot}10^5$ m^{-1}. The R_{th} data, extracted at 6.5 K, nicely fits with that of 75 K, giving continuity to the R_{th} curve. The thermal resistance curves, that are seen from the gate side, have the same shape as the thermal resistivity curve of Si. That confirms the hypothesis, that Si thermal resistance dominates over the other thermal components.

In addition to that, we performed the modeling of the $\Delta T - P$ behavior, based on the approach, proposed in [11]:

$$\delta\Delta T = R_{th}(T_A + \Delta T) \cdot \delta P \tag{2}$$

$$P = \int_0^{\Delta T} \frac{\delta\Delta T'}{R_{th}(T_A + \Delta T')} \tag{3}$$

Silicon specific resistance dependence over temperature multiplied by effective length versus area ratio, that serves as a fitting parameter, was taken as $R_{th}(T)$ function in (3). The result is shown in Fig. 9. The measured and calculated data agree with each other, and that additionally confirms our analysis above.

Thermal resistance, extracted at the gate side, shows noticeable dependence on bias voltages. As V_d increases from 0.5 to 2.0 V the $R_{th} - T$ curve shows a reduction in magnitude. It is especially clearly visible in the Fig. 10. The dependence on bias voltages most likely is a result of the influence of bias voltages on thermal embedding resistance of the transistor. Linear parts of the curves are parallel to each other in Fig. 10 (b) and have decreasing slope in Fig. 10 (a). That means, that V_d increase causes the decrease of thermal resistance. The dependence of the thermal resistance R_{th} on the linear parts of the curves in Fig. 10 (a) on V_{ds} for several T_A is shown in the Fig. 11. The slope of this dependency decreases with temperature. However, the reason of this thermal resistance decrease remains unclear and will be a subject of further studies.

IV. Conclusion

We introduced experimental results from a selfheating structure, fabricated using a commercial 65 nm TSMC CMOS technology. In this case the measurements were taken from a Si die attached with varnish glue to the cold plate of the cryostat. We have considered the four thermal paths determined by the bulk, source, drain, and gate (the passive thermal component). Due to the incorporation of different materials, such as the Si by itself with different doping levels, the SiO_2 and its interfaces with the channel and the gate, the polysilicon gate, the source and drain contact interfaces, and the glue used to attach the die to the cold plate, the thermal resistance is quite complex. The level of complexity increases when the local temperature actively changes with the bias condition. In highly integrated circuits, in turn, the nearby transistors will thermally interact with each other, changing each other's electrical behavior. This influence will be quite difficult to predict due to frequent change of dissipated power by each device.

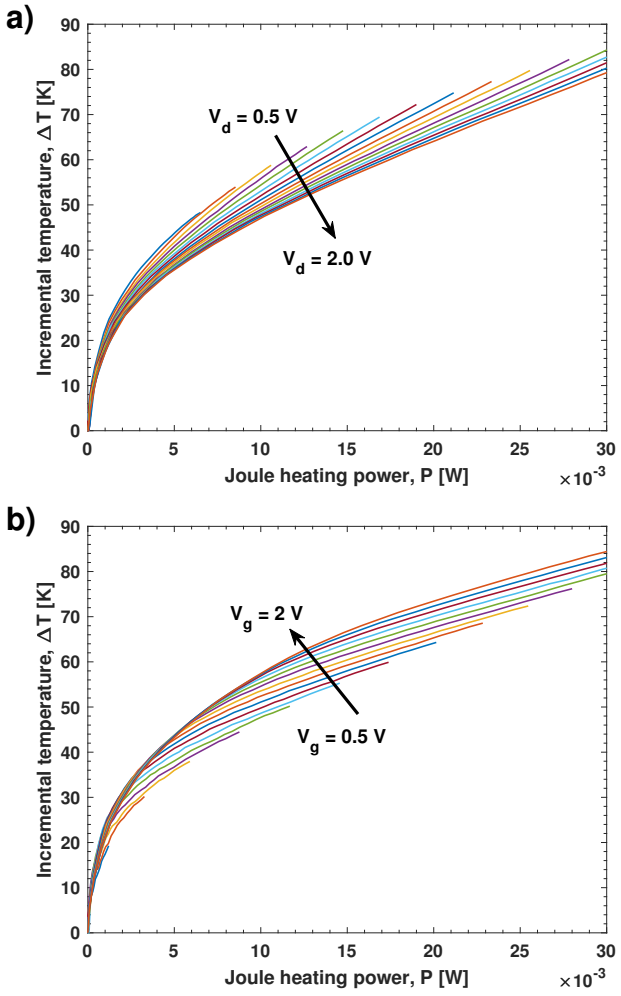

Fig. 10: The dependence of ΔT on Joule heating power P. V_g primary sweep and 0.1 V step V_d secondary sweep (a) and V_d primary sweep and 0.1 V step V_g secondary sweep (b).

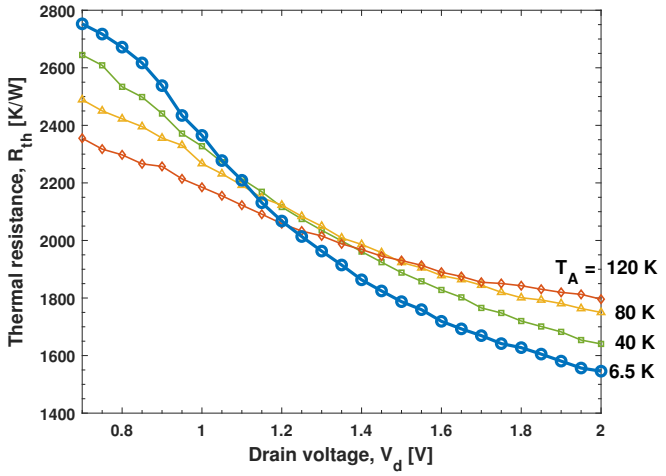

Fig. 11: Dependence of thermal resistance R_{th} (linear regime), seen from the gate side, on drain-source voltage V_d for several ambient temperatures T_A.

All this his prompts for the development of a thermal-de-embedding technique that enables the creation of dynamic or active thermal models for the CMOS technologies. These electro-thermal models should serve the purpose to reduce the thermal load, either by modifying the technology for specific cryogenic applications, such as bulk thinning or metal pillars in the bulk as heat exchangers, among other alternative approaches. Having a bias- and technology-dependent electro-thermal model should serve for the proper design of integrated circuits for cryogenic applications.

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